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(54) Computer equipped with plural processors.

(57) A loosely coupled multiprocessor computer (1) includes an input/output control unit (34, 35) for fetching both a program and data derived from an external input device and also for outputting processed data to an external output device; storage (32) for storing therein both the program and data inputted from said input/output control unit; process unit (33) for sequentially executing a processing operation of the data based upon the program stored in the storage; and, a transmission medium for coupling the process unit, input/output control unit and storage with each other. In the loosely coupled multiprocessor computer, a serial transmission medium (2) is employed as the transmission medium; transmission control unit (31) for performing both a conversion process between data to be transmitted, flowing through the serial transmission medium and the process d data, and also a transmission/reception process of the data to be transmitted via the serial transmission medium, is provided with the input/ output control unit, storage and process unit; and furthermore, unit process unit for controlling the input/output control unit, storage, and transmission control unit is provided with the input/output control unit and storage with the transmission control unit.

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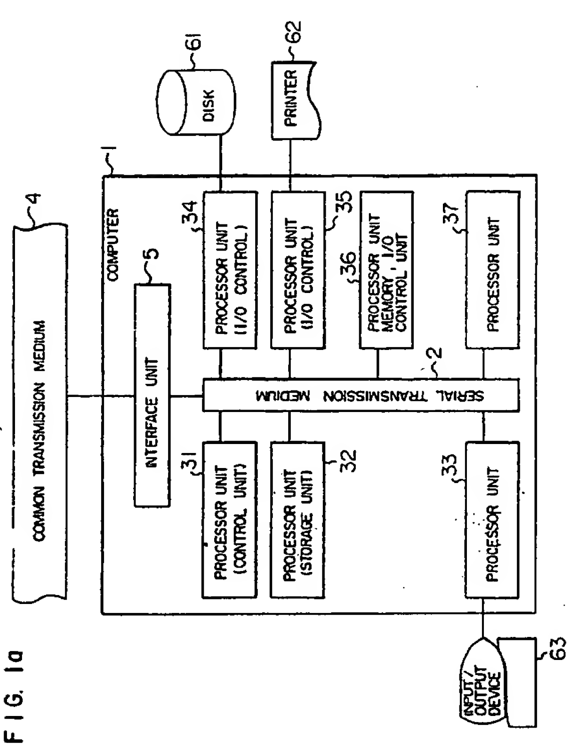

COMMON TRANSMISSION MEDIUM
4
COMPUTER
1
INTERFACE UNIT
5
PROCESSOR UNIT (CONTROL UNIT)
31
PROCESSOR UNIT (STORAGE UNIT)
32
PROCESSOR UNIT
33
SERIAL TRANSMISSION MEDIUM
2
PROCESSOR UNIT (I/O CONTROL)
34
PROCESSOR UNIT (I/O CONTROL)
35
PROCESSOR UNIT MEMORY, I/O CONTROL UNIT
36
PROCESSOR UNIT
37
DISK
61
PRINTER
62
INPUT/OUTPUT DEVICE
63

FIG. 1a

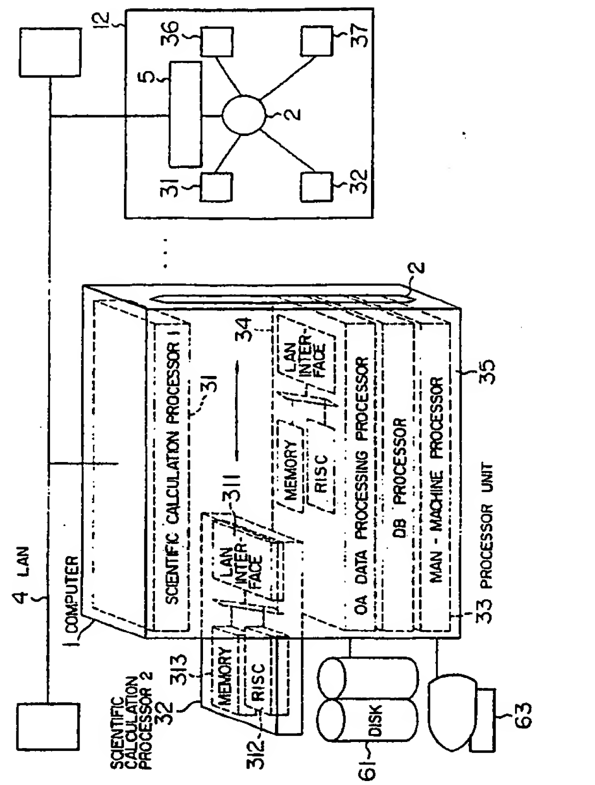

4 LAN
1 COMPUTER
SCIENTIFIC CALCULATION PROCESSOR 1
31
311
34
LAN INTER-FACE
MEMORY
RISC
LAN INTER-FACE
MEMORY
RISC
OA DATA PROCESSING PROCESSOR
DB PROCESSOR
MAN - MACHINE PROCESSOR
35
33 PROCESSOR UNIT
SCIENTIFIC CALCULATION PROCESSOR 2
32
313
312
DISK
61
63
2
12
5
36
37
31
32
2

FIG. 1b

COMPUTER EQUIPPED WITH PLURAL PROCESSORS

BACKGROUND OF THE INVENTION

The present invention generally relates to an architecture for both a hardware and a software used within a computer, and more specifically, to a computer including a loosely coupled multiprocessor.

Conventional computers have been developed and have progressed in such a manner that elements are highly integrated and physical distances among the elements are reduced as short as possible in order to increase processing speeds of these computers.

In Fig. 8, there is shown a schematic block diagram of a basic construction of the conventional computer.

A computer 80 includes as five major devices, a calculation device 81, a control device 82, a storage device 83, an input device 84, and an output device 85. Further, both the calculation device 81 and the control device 82 are incorporated into a central processing unit (referred to as a "CPU").

The computer 80 with the above-described construction executes the following operations.

First, a program is read out from the input device 84, and then is stored into a program region within the storage device 83. The control device 82 sequentially reads out the programs stored with this storage device 83 one by one so as to be decoded, and thereafter sends various instructions to the input device 84, output device 85 and storage device 83 which are required to execute commands written in the programs.

When, for instance, the command of the program corresponds to a command (READ command and the like) for requesting a data input, the inputted data is stored into an input region within the storage device 83.

Also, when the decoded command corresponds to a calculation command, data to be calculated is sent to the calculation device 81 in which a predetermined calculation is carried out.

Furthermore, data to be outputted is stored into an output region of the storage device 83. In response to an output command (WRITE command), the data stored in this output region is outputted by utilizing the output device 85.

As previously described, the computer 80 fetches the commands stored in the storage device 83 one by one, and executes processing operations in accordance with the programmed sequence.

Various system arrangements have been proposed in order to increase reliabilities of the computer systems with employment of such computers.

Among these computer systems, there is a multiprocessor system. In accordance with the multiprocessor system, a plurality of processors (processing device including CPU as an element) constitute a system for commonly using a main storage device and a file. When malfunction happens to occur, if only failed devices, processors, or a troubled unit employed within the main storage device are isolated from the computer system, the computer system may continue the processing operations, although the processing capabilities of the data are lowered. As a consequence, such a multiprocessor computer system owns better adaptability and therefore is suitable for constituting a large-scale on-line computer system.

This multiprocessor system may be further understood as one of parallel-processing computer systems.

"Parallel processing" operations imply that processing operations which have been performed by a single processor employed within the conventional computer, are performed in a parallel form by parallel-operating plural processors. As a result, highspeed processing operations may be realized.

As to the parallel processing operation, it may be subdivided into SIMD (Single Instruction Multiple Datastream; a single instruction and plural data method), and MIMD (Multiple Instruction Multiple Datastream; a plural-instruction and plural data method), depending upon arrangements of processors and processing ways.

The "SIMD" method is such a method that a plurality of processors execute plural data in synchronization with each other in response to the same instruction supplied from a central control device. Since each of the processors can parallel-execute the same instruction in this SIMD method, this method is suitable for such a case that similar types of calculations are performed for a large quantity of data.

In accordance with the MIMD method, on the other hand, each of the processors is independently operable, and a plurality of data processing operations are executed in an asynchronization mode in response to a plurality of different instructions. Since the respective processors are separately operated, control functions are provided within these processors. Also, communication networks to perform information exchanges among the respective processors are provided, which is similar to that of the SIMD method.

Fig. 9 is a schematic block diagram for representing a system arrangement of the MIMD meth-

od.

A processor (1) 911, a processor (2) 912, and a processor (n) 913 include an ALU (arithmetic logic unit) 914, a storage unit 915, a control unit (1) 914, a control unit (2) 917, and further a control unit (n) 918, respectively, and are connected to either a coupling network, or a shared memory 918.

A multiprocessor system corresponds to one of this MIMD method, and is so constructed that a large number of processors closely communicate with each other with employment of a highspeed coupling network and are operable in a parallel mode with better cooperation.

Then, the multiprocessor system is roughly categorized into two communication methods effected among the processors.

(a) Multiprocessor sharing memory.

Each of processors is operable with sharing a main storage device. The main storage device may be directly accessed by an instruction of the respective processors. If all of storage domains are completely shared, the access traffic to the main storage device becomes large, whereas when the number of the processors is increased, a bottleneck happens to occur and thus performance of the multiprocessor is degraded.

As a consequence, there are many possibilities to employ the following methods.

(i) Each of processors is equipped with own local memory, the access of which does not compete with the accesses of other processors, and a shared region is limited to a portion.

(ii) Each of processors is equipped with a cache memory.

(iii) A shared memory domain is subdivided into a plurality of partial domains, which will be allocated to each processor.

A memory shared type multiprocessor corresponds to a tightly coupled multiprocessor, and the total number of processors is suppressed due to the accessing contention to the shared memory, and therefore becomes small normally.

(b) A message exchange type multiprocessor.

Communications among processors are performed via I/O ports in a message communication mode. A packet communication method and the like are employed. The message exchange type multiprocessor corresponds to a loosely coupled multiprocessor. The total number of the processors may be selected to be greater than that of the above-described memory shared type multiprocessor, depending upon the communication network condition and applications.

In general, conventional computers have been progressed by improving the processing capabilities including the reliabilities. The processing speeds of the elements employed in the conventional computers are tried to be increased, and on the other hand, the processing capabilities are improved by the computer system arrangements. Among these improvements, there is one improving method, i.e., a parallel processing operation by multiprocessor systems.

In the processors employed in the conventional processor system, the data and control signal communications are performed via the parallel bus within the processors.

That is to say, each of units is connected via an internal bus to each other, which is similar to the normal computer.

In Fig. 9, for instance, various signals are mutually transmitted/received via the internal bus among the ALU 914, storage unit 915 and control unit (1) 915 employed within the processor (1).

As previously described, since the respective processors employed in the multiprocessor system are operable similar to those of the normal computer, when, for instance, the storage unit 915 in the processor (1) 911 is brought into malfunction, the power source of the processor (1) 911 is turned off, whereby the failed storage unit 915 is repaired.

Also, even when the function of the processor (1) 911 is expanded, the power source of this processor (1) 911 is once turned off and thereafter must be isolated from the multiprocessor system.

As previously explained, no specific care has been taken into such expansion and maintenance of the processor per se in the conventional computer system. Therefore, the processing operation required for each of the processors must always be carried out, taking account of the functions and processing operations of other processors. To mutually operate these processors, complex and large-scale management softwares are necessarily required, which may result in lowing the performance of the computer system.

In addition, when malfunction of processors happens to occur, the malfuncting processors must be isolated from the entire system and therefore the processing capabilities of the computer system are deteriorated.

SUMMARY OF THE INVENTION

An object of the present invention is to solve these problems of the conventional computer systems, and to provide such a computer capable of loosely-coupling a CPU and various devices such as storage devices employed in a computer so as to establish a loosely coupled hardware architecture, whereby the respective devices are mutually operable on the loosely couple hardware architec-

ture in order to perform a parallel processing operation at a higher speed; and also capable of performing maintenance as well as expansion processing operations of the computer, while continuing the computer processing operations.

To achieve such an object, a computer, according to the present invention, constructed of a plurality of processors, these processors being stored within a single housing, has a serial transmission medium employed as a common transmission medium for coupling the processors.

Furthermore, a computer, according to the present invention, where a plurality of computer units are connected with each other via a transmission medium, is featured in that at least one of these computer units is arranged by a plurality of processors, and also these processors are mutually connected via a serial transmission medium.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1a is a schematic block diagram for representing a preferred embodiment of a computer according to the present invention;

Fig. 1b schematically illustrates an example of a computer mounting construction according to the present invention;

Figs. 2a to 2d are schematic block diagrams for showing internal arrangements of the computer shown in Fig. 1;

Fig. 3 is a schematic block diagram of an arrangement of a computer employing an optical fiber as a serial transmission medium shown in Fig. 1;

Fig. 4 is a schematic block diagram for showing a simple construction of a multiprocessor system employing the computer shown in Fig.

Fig. 5 is an illustration for explaining a data format 11 transferred/received via the serial transmission medium shown in Fig. 1;

Fig. 6 is a schematic block diagram for representing an internal arrangement of an interface unit shown in Fig. 1;

Fig. 7 is a schematic block diagram for representing an arrangement of a multiprocessor system employing the computer shown in Fig. 7;

Fig. 8 is a schematic block diagram for showing a basic arrangement of the conventional computer;

Fig. 9 is a schematic block diagram for representing a construction of the MIMD system;

Fig. 10 is a schematic block diagram for representing a computer according to another preferred embodiment of the present invention;

Fig. 11 is a schematic block diagram for showing a system in which a plurality of computers shown in Fig. 10 are connected to each other;

Fig. 12 is a schematic block diagram for representing an internal arrangement of the computer shown in Fig. 10;

Figs. 13 and 14 are schematic block diagrams for representing an internal arrangement of a computer according to a further preferred embodiment of the present invention;

Fig. 15 is a schematic block diagram of a software executed on an internal arrangement of the computer shown in Fig. 10; and,

Fig. 16 is a schematic block diagram for explaining that an optical transmission medium is employed as the serial transmission medium within the computer shown in Fig. 10, and is detachably connected with the transmission medium of the processor.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Various preferred embodiments according to the present invention will now be described with reference to drawings more in detail.

Fig. 1a is a schematic block diagram of an circuit arrangement of a computer according to a preferred embodiment of the present invention.

A computer 1 is so arranged by a plurality of processor units 31 to 36; a serial transmission medium 2 for connecting these processor units with each other; and an interface unit 5 for interfacing the serial transmission medium 2 and a common transmission medium 4 used to connect other computers therewith. Then, the computer 1 is connected via the common transmission medium 4 to other computers (not shown).

In general, this serial transmission medium 2 corresponds to a transmission medium employed in a network, is made of an optical fiber, a coaxial cable, a twisted pair line.

The processor units 31 to 36 are constructed as a storage unit, a control unit and the like, respectively and have such a basic arrangement of an interface unit with the serial transmission medium 2 and a control function as the processor unit.

The processor unit 31 corresponds to the control unit having a function as a control section in the computer 1, whereas the processor unit 32 corresponds to the storage unit having a memory.

The processor unit 33 owns a function for interfacing an input/output device and therewith, is connected to an external input/output device 63. Similarly, the processor unit 34 is connected to an external disk 61, and the processor unit 35 is connected to a printer 62.

Then, the processors 36 and 37 are equipped with a memory and an I/O control section, and have functions as a single independent computer.

It should be noted that this arrangement shown in Fig. 1 is merely one example, and therefore the present invention is not limited to this arrangement. That is to say, the combinations between the pro-

cessor units and internal arrangements of the processor units, and also quantities thereof may be freely changed in accordance with purposes. Similarly, it should be understood that the below-mentioned processing operations are merely an example, and when the internal arrangements of the processor units, combinations between the processor units and also quantities thereof are changed so as to newly perform another processing operation, a computer constructed of these processor units may execute a desirable processing operation.

Fig. 1b is an illustration for showing one example of a mounting structure for the computer shown in Fig. 1a according to the present invention.

In this figure, the computer 1 is constructed of the processor units 31 to 35 installed within a single housing, and also the serial transmission path 2 installed within this housing. In Fig. 1a, there is shown a LAN (Local Area Network) employing an optical fiber as the serial transmission path 2. Each of these processor units is so constructed that, as shown in the processor unit 32, these processor units may be detachably connected to this LAN 2 and housing. Connectors (not shown) employed at a LAN interface unit for the processor unit and also at the LAN 2 are employed to connect/disconnect the respective processor units. An internal arrangement of the respective processor unit is constructd of a calculation processing section (RISC) 312 and a memory 313 other than a LAN interface section 311, as will be discussed later.

In the example of Fig. 1b, the computer 1 stored in this single housing is further connected via the common transmission medium 4 externally provided to another computer 12. Alternatively, the computer 1 may be solely employed. It should be noted that although not shown in Fig. 1b, the LAN 2 is connected via the interface unit to the computer.

The computer 1 with the arrangement shown in Fig. 1a will perform the following operations.

A command inputted from the input/output device 63 is processed in the processor unit 33. In case that this command processed in the processor unit 33 is to instruct execution of a certain program; data for instructing the execution of this program is transferred to the serial transmission medium 2. When this program has been stored in, for instance, the disk 61, the processor unit 34 fetches the above-described data from the serial transmission medium 2, and transfers this program to the serial transmission medium 2. The processor unit 31 for executing a control of a program receives the program as data from the serial transmission medium 2, and perform the processing operation thereon. As a result of this processing operation, when, for example, an output to the input/ output device 63 is required, this processed result is sent as the data to the serial transmission medium 2. This data is fetched by, for instance, either the processor unit 33 or 35, and then outputted to either the input/output device 63 or printer 62.

It should be noted that a transmission procedure or sequence for transmitting/receiving data via the serial transmission medium 2, which has been produced by the above-described series of data processing operation, is performed in accordance with a proper transmission procedure (will be described later).

Data transmission/reception among the units the performed via the serial transmission medium 2 with each other.

It should also be noted that a series of data processing operations may be executed by employing the processor units 36 and 37.

Then, the computer 1 is connected via the interface unit 5 to the common transmission medium 4, and performs a data processing operation in parallel with a similar computer (not shown) connected to this common transmission medium 4.

As described above, each of the function processor units employed within the computer 1 shown in Fig. 1 is connected via the serial transmission medium 2 to each other, the data transmission/reception among the processor units are performed via this serial transmission medium 2. As a consequence, neither shared memory, nor system bus is present in the computer, which is similar to the conventional multiprocessor, so that these processors are loosely coupled with each other in view of hardware and software.

Since the respective processor units are loosely coupled with each other, the computer 1 may be constructed by freely combining a plurality of processors having various functions, and therefore may be realized as a loosely coupled multiprocessor computer.

Even when, for instance, another processor unit is additionally employed so as to expand a function, and maintenance of a single processor is carried out, expansion and maintenance processing operations may be executed without interrupting a power supply of the computer 1, while performing the processing operations.

In other words, the processor units may be connected/disconnected within the computer in a unit of a single processor unit without interrupting the operations of the computer.

It should be noted that the transfer control for transmitting/receiving data via the serial transmission medium 2 may by performed based upon a previously determined transfer protocol.

Also, this transfer control method may be realized by utilizing the protocol of the conventional

LAN (Local Area Network) and conventional apparatuses. In this case, this transfer control function is realized by an interface section with the serial transmission medium 2. Generally speaking, this interface section corresponds to an LAN adapter.

Otherwise, an optical fiber may be employed as the serial transmission medium 2, as will be discussed later.

Since the same operating systems (i.e., software management program) operable on the respective processor units in the computer 1 are employed, compatibility or interchangeability among these processor units may be established and the interchanging operation as well as the processing operation for the expansion may be easily performed.

Fig. 2 is a schematic block diagram for showing an example of an internal arrangement of a processor unit for the computer shown in Fig. 1.

Fig. 2a represents an internal arrangement of the processor unit 31, in which a transmission control section 311 functioning as an interface with the serial transmission medium 2 and the processor unit 31 is connected to a CPU (central processing unit) 310 via an internal bus 315.

The CPU 310 controls an overall operation of the computer 1 shown in Fig. 1. The transmission control section 311 performs the data transmission/reception between the processor 310 and processors employed within other processor units through the serial transmission medium 2.

The processor unit 31 owns such a function as the central processing unit (CPU) in the conventional computer.

In Fig. 2b, there is shown an internal arrangement of the processor unit 32, in which a memory 313 is connected via an internal bus 315 to both the transmission control unit 311 and a unit CPU 312. This memory 313 is operated under control of the unit CPU 312 and owns a function as the storage device in the conventional computer.

Fig. 2c represents an internal arrangement of the processor unit 33. An I/O control section 314 is connected via an internal bus 315 to the transmission control section 311 and unit CPU 312. As represented in Fig. 1, the input/output device 63, disk 61 and printer 62 are connected via this I/O control section 314, which is completely similar to the constructions of the processor unit 34 and 35 shown in Fig. 1.

The processor unit 33 is operated under control of the unit CPU 312, and has such a function as the input/output device in the conventional computer.

Fig. 2d indicates an internal construction of the processor unit 36. The processor unit 37 shown in Fig. 1 has the similar internal arrangement, and the processor unit 36 has a function as a single computer. That is to say, both a memory 313 and I/O control section 314 are connected via an internal bus 315 to a transmission control unit 311 and a unit CPU 312. Further, a disk 316 as an internal storage medium is connected the I/O control section 314.

It should be noted that this disk 316 may be provided outside the computer 1 shown in Fig. 1, which is similar to the disk 61 of the processor unit 34. Moreover not only the disk, but also the input/output device or printer may be connected thereto.

As previously described, the processing operations are carried out by utilizing the program and data stored in the memory 313 or disk 316 by way of the unit CPU 312 in the processor unit 36. The processor unit 36 receives the data derived from other processor units via the serial transmission medium 2 and also sends out the data of the own processor unit to other processor units, if required.

As a result, the computer 1 shown in Fig. 1 may execute a plurality of processing operations with respect to a single job by mutually operating the respective processor units.

It should be understood that the connection arrangements shown in Fig. 2 are merely represented as examples for the computer 1, and therefore may be readily modified in accordance with the desirable function.

As previously described, the independent processor units are so connected to the serial transmission medium 2 within the computer 1 shown in Fig. 1, whereby the computer 1 is realized as a loosely coupled multiprocessor computer.

Fig. 3 is a schematic block diagram for representing an arrangement of a computer when an optical fiber is employed as the serial transmission medium shown in Fig. 1.

In other words, the serial transmission medium 2 of the computer 1 shown in Fig. 1 is realized by an optical fiber.

To connect each of processor units to a serial transmission medium 2 made of an optical fiber, both an OE converter 317 and an optical connector 318 are additionally employed.

The OE converter 317 converts an electric signal processed in the transmission control section 311 into an optical (laser light) signal, whereas the optical connector 318 optically connects the OE converter 317 with the serial transmission medium 2 made of an optical fiber.

Each of the processor units may be disconnected from computer 1 with employment of this optical connector 318, so that the maintenance and expansion processing operations may be performed without interrupting the computation by the computer 1.

More specifically, since the optical fiber is em-

ployed and the connection/disconnection of the processor units are realized at the optical connector units, it may be prevented that electric arc and the like happen to occur due to the electrical connection/ disconnection of the processor units. As a consequence, the electrical connection/disconnection of the processor units during the maintenance and expansion may be more safety carried out even when the computer 1 is under operation.

Fig. 4 is a schematic block diagram for showing a simple construction of a multiprocessor system employing the computers shown in Fig. 1.

The respective computers 11 to 13 each having the same arrangement as that of the computer shown in Fig. 1 are connected via a common transmission medium 4 to each other, which is completely similar to the conventional multiprocessor system.

With this arrangement, each of the computers 11, 12 and 13 may perform the parallel processing operation, which is similar to that of the conventional computer.

Furthermore, if, for instance, the functions of a computer are expanded in the conventional computer system, the power source of this computer must be turned off to cease the functions of the computer before the expansion should be carried out. However, in the computer 11 according to the loosely coupled multiprocessor computer of the present invention, since the function related only to the expansion processing operation may be interrupted, the processing operations for the multiprocessor system may be continuously carried out.

Next, the data transmission procedure executed among the processor units via the serial transmission medium 2 shown in Fig. 1 will now be explained.

Fig. 5 schematically illustrates a format of data which are transmitted/received via the serial transmission medium shown in Fig. 1.

The data 600 is constructed of a content code 601 representative of a content of the data, a control code 602, and a data unit 603.

In Fig. 1, when data is transmitted from the respective processor units to the serial transmission medium 2, the content code 601 is set into this data. This data is broadcasted (reported) via the serial transmission medium 2 to other processor unit. While investigating the content code 601 of the data flowing through this serial transmission medium 2, each of these processor units may fetch only data which must be required for own processor unit.

Which content code of the data to be fetched, has been set into the transmission control unit 311 in the respective processor units.

Subsequently, the interface unit 5 of the computer 1 will now be described.

Fig. 6 is a schematic block diagram for showing an internal arrangement of the interface unit 5 represented in Fig.

An interface section 501 for interfacing the serial transmission medium 2 and therewith, an interface section 502 for interfacing the common transmission medium 4, and a memory 503 and also a unit CPU 312 are connected via an internal bus 504 to each other.

The interface section 501 corresponds to a transmission control unit 311 shown in Fig. 2. As previously stated, the construction of the interface unit 5 is similar to that of each of the processor units shown in Fig. 1. The interface unit 5 may be regarded as the processor unit which executes the data transmission/reception among the computers under the control of the unit CPU 312.

The interface unit 5 with the above-described construction may be operated as an interface for interfacing the common transmission medium 4 for coupling the computers which perform the parallel processing operations, and the serial transmission medium 2 for coupling the processor units within the computer.

That is to say, the data flowing through the serial transmission medium 2 is received by the interface section 501 and transmitted via the internal bus 504 employed in the unit to the interface section 502, if required. The interface section 502 sends out the data derived from the interface section 501 to the common transmission medium 4.

On the other hand, the data flowing through the common transmission medium 4 is fetched by the interface section 502, and then transferred to the interface section 501, if necessary, and to the serial transmission medium 2.

The memory 503 temporarily stores (buffers) data to be transmitted and/or received, and is used as a storage area for a program and data which are utilized to be processed in the interface sections 501 and 502.

As previously described, the structure of this interface unit 5 is, in principle, the same as that of each of the processor units shown in Fig. 1. As to the transmission function via the serial transmission medium 2, both the interface unit 5 and processor unit have the similar functions. In this interface unit 5, an application process may be executed and the I/O control section 314 (refer to Fig. 2c) may be employed.

It should be also noted that the structure of the common transmission medium 4 for coupling the computers may be the same as that of the serial transmission medium 2, and furthermore may be constructed of a normal LAN (Local Area Network). In this case, the interface unit 5 has such a function corresponding to a so-called "bridge" device in

LAN.

Fig. 7 schematically represents a structure and an operation of the multiprocessor system employing the computer shown in Fig. 1.

This figure represents such a condition that the data flowing through a single computer and plural computers are transmitted and/or received among the processor units employed in the respective computers.

In particular, this figure represents such a case that a data transmission method with a content code for describing a method to transmit/receive data is utilized.

Transmission data of a single processor unit, for instance, the processor unit 31 is first broadcasted via the serial transmission medium 21 within the computer 11 including this processor unit 31.

It is possible to determine the data transmission sequence between the computers 11 and 12 via common transmission medium independent of the data transmission sequence between processors via serial transmission medium in a computer. Also, a normal LAN may be employed.

Even in the computers, when the data transmission/reception are carried out with employment of the data having the content code, for instance, the interface unit 51 within the computer receives the data which has been broadcasted via the serial transmission medium 21 and broadcasts this data to the common transmission medium 4 among the computers. Then, the interface unit 52 within the computer fetches the data which has been broadcasted via the common transmission medium 4, and the computer 12 broadcasts this data to the serial transmission medium 22 within the computer.

The way to setting the content code may be determined freely for data transmitted between computers and also for data transmitted between processors of a computer. The both codes may be the same in accordance with their protocols. In case of the same setting method, the data flowing through the computer directly flows among the computers. Also, in case of the different setting methods, the content codes are substituted with each other in the interface units 51 and 52. This substitution is made by deleting one content code from data and adding the other code instead thereof to the data.

As previously explained, in accordance with the preferred embodiments of the present invention, since the processor units within the computer are loosely coupled with each other, the processor units may be connected/disconnected under online condition of the computer system. As a consequence, to improve the processing capabilities as well as the reliabilities of the computer, the functions may be expanded and also the maintenance of the computer may be carried out without interruption of the computer jobs which have already been operated when a user makes his command.

Furthermore, since the processing capabilities, functions and reliabilities of the computer may be controlled by adjusting the quantity of the processor units built in this computer, every user need not establish a series of computers with various grades, but also need not replace the computer with a single computer unit.

In addition, the overall system of the computer need not be interrupted during maintenance of the computer system, especially the version-up of the software such as the operating system, and therefore maintenance required for a portion of the computer system may be independently executed in the overall computer system.

Also, since the loads on the computer may be distributed to a plurality of processor units within the computer, the overall processing capabilities of the computer system may be increased.

Thus, if the processor units within the computer include only the interfaces with the serial transmission medium, then these processor units may communicate with each other, so that these processor units may be constituted as a multiprocessor, irrelevant to the model of the processor units and also the operating system for the processor units.

In addition, since the function distribution and load distribution may be realized within a single computer, these function/load distributions do not depend upon either the computer setting place, or computer user. Namely, the number of processors included in a computer may be changed without stopping user's programs in response to requirement of load distribution in the whole system. To the contrary, when the function/load are distributed among the computers, these load/function distributions depend upon the computer setting place and/or computer user.

Moreover, since only the specifically restricted processing operations are performed by the respective processor units within the computer, and also these specifically restricted processing operations are combined with each other so as to execute a single job, the operating systems for managing the softwares of the respective processor units may be simplified, resulting in lower cost.

Fig. 10 is a schematic block diagram of a computer system according to another embodiment of the present invention.

A computer 11 is constructed of a plurality of processor 31 to 37 and a common transmission medium 2 for coupling the processors set within this computer. It should be noted that the common transmission medium 2 corresponds to a serial

transmission medium utilized in a network communication and a wireless communication. The computer 11 is coupled via a common transmission medium 41 for coupling the computers to another computer 12. The processors 33 to 36 own an interface function with an external apparatus (external input/output apparatus), and are connected to each of disk device 61, printer device 62, terminal device 63, and communication line (trunk) 42. Information (data) transmission/ reception among the processors are performed only through the serial transmission medium 2. Neither a system bus nor a shared memory is provided among the processors, which is similar to the conventional multiprocessor. The processor 37 is mutually connected to the serial transmission medium 2 and common transmission medium 41, and performs a process to relay one information (data) flowing through one transmission medium to the other information (data) flowing through the other transmission medium. The processor 36 is also connected to the communication line 42 functioning as one common transmission medium. However, this communication line 42 corresponds to the external device for the processor 36. As a consequence, the information which is transmitted/received via the communication line 42 to/from another computer 14, is utilized so as to be processed in the processor 36.

It should be understood that both the sorts of the processors and quantities thereof corresponding to the constructive element of the computer according to the preferred embodiment do not define the internal constructive element of the computer 11, but may be selected in conformity to the utility of this computer 11, and the processors are connected to the serial transmission medium. As a consequence, for instance, only necessary external devices may be connected to the corresponding processors, which may therefore constitute the external device of the computer 11. In other words, the computer 11 may be constructed by arbitrarily combining the processors having the various functions.

Fig. 11 is a schematic block diagram of another preferred embodiment in which a plurality of computers 11 to 13 are connected with each other via a common transmission medium. It should be noted that both the computer 12 and 13 may be constructed of either the computers using the inventive system, or the conventional computers. The computer 11 using the inventive system may transmit and receive the information via the common transmission medium 41 to and from other computers.

Fig. 12 is a schematic block diagram for showing an example of an internal arrangement of the processors to constitute the computer 11. A processor 31 is arranged by a transmission control section 311 functioning as an interface with the serial transmission medium 2, a calculation processing section 312, and a local memory 313 of the calculation processing section 312. A processor 32 has a structure similar to that of the processor 31, and is constructed of a transmission control section 311, a calculation processing section 322, and a local memory 323 for the calculation processing section 322. It should be noted that the internal arrangements of these processors 31 and 32 need not be exclusively designed to the arrangement shown in Fig. 3, except that these processors own the interface with the serial transmission medium 2. Fig. 13 illustrates an example in which a processor includes an interface section 334 for interfacing an external device 61 (external input apparatus) of a computer and therewith. As this external device 61, i.e., a disk device, a printer device, a terminal device (CRT, keyboard), and a line may be freely employed.

Also, as represented in Fig. 14, it should be noted that calculation processing sections 342, 352 and local memories 343, 353 may be different from each other in each of the processors 134 and 135. That is to say, it is known that various types of conventional calculation processing sections and local memories have been commercially available. If these elements own the interface function with the serial transmission medium, these elements may be employed as the constituting elements of the processors. For instance, the processing method of the calculation processing section, the processing speed, the word length, the accessing method of the local memory, the memory capacity of the local memory and the like may be different from each other in the respective processors. It should be noted that these calculation processing section and transmission control section 311 are connected to each other via internal buses 344 and 354.

Fig. 15 is a schematic block diagram for representing a functional structure of a program (software) operated on each of processors 36 and 37. Reference numerals 361 and 371 indicates a transmission control program by which information transmission/reception are carried out via a serial transmission medium to other processors. Reference numerals 362 and 372 represent system programs (operating systems) for managing application programs 363 and 373 executed in the respective processors 36 and 37. Each of the system programs 362 and 372 owns transmission control programs 361 and 371 and an interface, and each of these control programs performs the information transmission/reception among other processors.

This information transmission and reception are realized in conformity with the data format shown in

Fig. 5. It is assumed that a concrete attribute (data length, sort of data code) of the data format is previously determined. Each of the processor units performs the information transmission/reception in conformity with this data format. As previously stated, in case that LAN corresponding to prior art is employed as the serial transmission medium 2, the data format should be defined in accordance with that used in prior art.

The processing operations performed in the respective processor units are independently carried out with respect to those of other processor units, other than the processing operation of the information transmission/reception via the serial transmission medium. As previously described, the sorts of the processors and of the operating systems may be different from each other. Only when one process for transmitting the data on the processing result at this processor unit to the serial transmission medium, and also the other process for fetching the data from this serial transmission medium are carried out, a conversion process is executed between the above-described data format which has been totally determined and the format of the respective processor units. This conversion process is performed by the transmission control section.

As previously represented, the transmission control sequence for transmitting/receiving the information is performed based upon a predetermined proper sequence.

Fig. 16 is a schematic block diagram for representing the transmission control sections 311 of the processor more in detail. Fig. 16 is such an example where an optical transmission medium is employed as the serial transmission medium 2. Each of the transmission control sections 311 is constructed of connection sections (connector sections) 3111, 3112 with the optical transmission medium, an opto/electric converting section 3113, and a transmission control processing section 3114. The connection sections 3111 and 3112 correspond to connectors. Light cannot be transferred to the part 3112 by disconnecting the part 3111 from the part 3112. Under such a disconnecting state, when the part 3111 is connected to the part 3112, the light can be transferred to the part 3112. When this mechanism is incorporated into the processors, each of these processors may be connected/disconnected to the serial transmission medium. In other words, the processors for constituting the computer may be connected/disconnected, if required. Since the connecting/disconnecting parts correspond to optical interface parts, there is no risk that short circuit and discharge phenomena happen to occur, as in the electrical interface parts. As a result, each of the processors may be connected/ disconnected to/from the computer system, while operating all of the processors. In other words, there is no adverse influence given to the hardwares of the processor units and serial transmission medium, when these optical interface units are connected/disconnected.

On the other hand, as previously described, the adverse influence given to the software operable on the processor units may be avoided by setting a function such as the conventional LAN to the serial transmission medium. For instance, as the conventional token ring LAN, an automatic mechanism control function may be set to the serial transmission medium, by which the information transmission/reception among the computers coupled to this token ring LAN are guaranteed when the transmission control apparatus is connected/disconnected to/from the computer system.

Claims

1. A computer (1) comprising:
a plurality of processors (31-37); and,
a serial transmission medium (2) for coupling said plurality of processors, both said processors and serial transmission medium being stored within a single housing.

2. A computer system in which a plurality of computers (11-13) are connected via a transmission medium (4) with each other, wherein:
at least one of said computers comprises a plurality of processors (31-37) and a serial transmission medium (2) for coupling said processors to each other.

3. A computer as claimed in Claim 1, wherein each of said processors includes:
means for fetching from the serial transmission medium, at least a portion of information required to execute a program operated on said processor; and,
means for detecting whether or not the information required to execute said program has been prepared, for initiating said program so as to execute a processing operation when said information has been prepared, said prepared information being used as input information, and also for sending out information which is outputted from said program as a result of the execution, to said serial transmission medium, whereby a series of processing operations related to a single job are performed by mutually operating said plurality of processors.

4. A computer as claimed in Claim 3, wherein each of said processors includes an operating system for managing the execution of the pro-

gram operated on the processor.

5. A computer as claimed in Claim 4, wherein different sorts of operating systems operated on each of the processors are employed.

6. A computer as claimed in Claim 3, wherein a predetermined transmission sequence is utilized so as to transmit/receive the information via said serial transmission medium among said processors.

7. A computer as claimed in Claim 6, wherein as the transmission sequence of the information performed via said serial transmission medium among the processors, such a method is employed that when each of said processors sends out said information to said serial transmission medium, a content code indicative of a content of said information is attached to said information, and when each of said processors receives said information, each of said processor judges whether or not said information is required by checking said content code.

8. A computer as claimed in Claim 1, wherein an optical medium is employed as said serial transmission medium.

9. A computer as claimed in Claim 7, wherein an interface section is connectable/disconnectable between said optical medium and said processor.

10. A computer as claimed in Claim 3, wherein each of said processors performs a management of an input device, an output device, and a memory device employed in said computer, and a series of processing operations related to a single job which is executed with employment of said devices, are carried out by mutually operating said plurality of processors.

11. A computer as claimed in Claim 1, wherein said devices employed in the computer are connected/disconnected to/from said serial transmission medium either at a time instant where said devices are required, or at a time instant where said devices are no longer required.

12. A loosely coupled multiprocessor computer in which there are provided:
input/output control means for fetching both a program and data derived from an external input device and also for outputting processed data to an external output device;
storage means for storing therein both the program and data inputted from said input/output control means;
process means for sequentially executing a processing operation of said data based upon the program stored in said storage means; and,
a transmission medium for coupling said process means, input/output control means, and storage means with each other, wherein:
a serial transmission medium is employed as said transmission medium;
transmission control means for performing both a conversion process between data to be transmitted, flowing through said serial transmission medium and said processed data, and also a transmission/reception process of said data to be transmitted via said serial transmission medium, is provided with said input/output control means, storage means and process means; and furthermore,
unit process means for controlling said input/output control means, storage means, and transmission control means is provided with the input/output control means and storage means on which said transmission control means.

13. A loosely coupled multiprocessor computer as claimed in Claim 12, wherein an optical fiber is employed as said serial transmission medium.

14. A loosely coupled multiprocessor computer as claimed in Claim 12, wherein a plurality of processor units constructed of said input/output means, unit process means, transmission control means, and storage means are employed so as to perform a series of process operations related to a single job under condition that these process operations are distributed by said plurality of processor units, and also so as to constitute a multiprocessor system for transmitting/ receiving data required for the process operations via said serial transmission medium connecting said processor units, and mutually performing the process operations in said plural processor units.

15. A loosely coupled multiprocessor computer as claimed in Claim 12, further comprising:
a protocol for previously determining a transmission control method of a data transmission effected via said serial transmission medium.

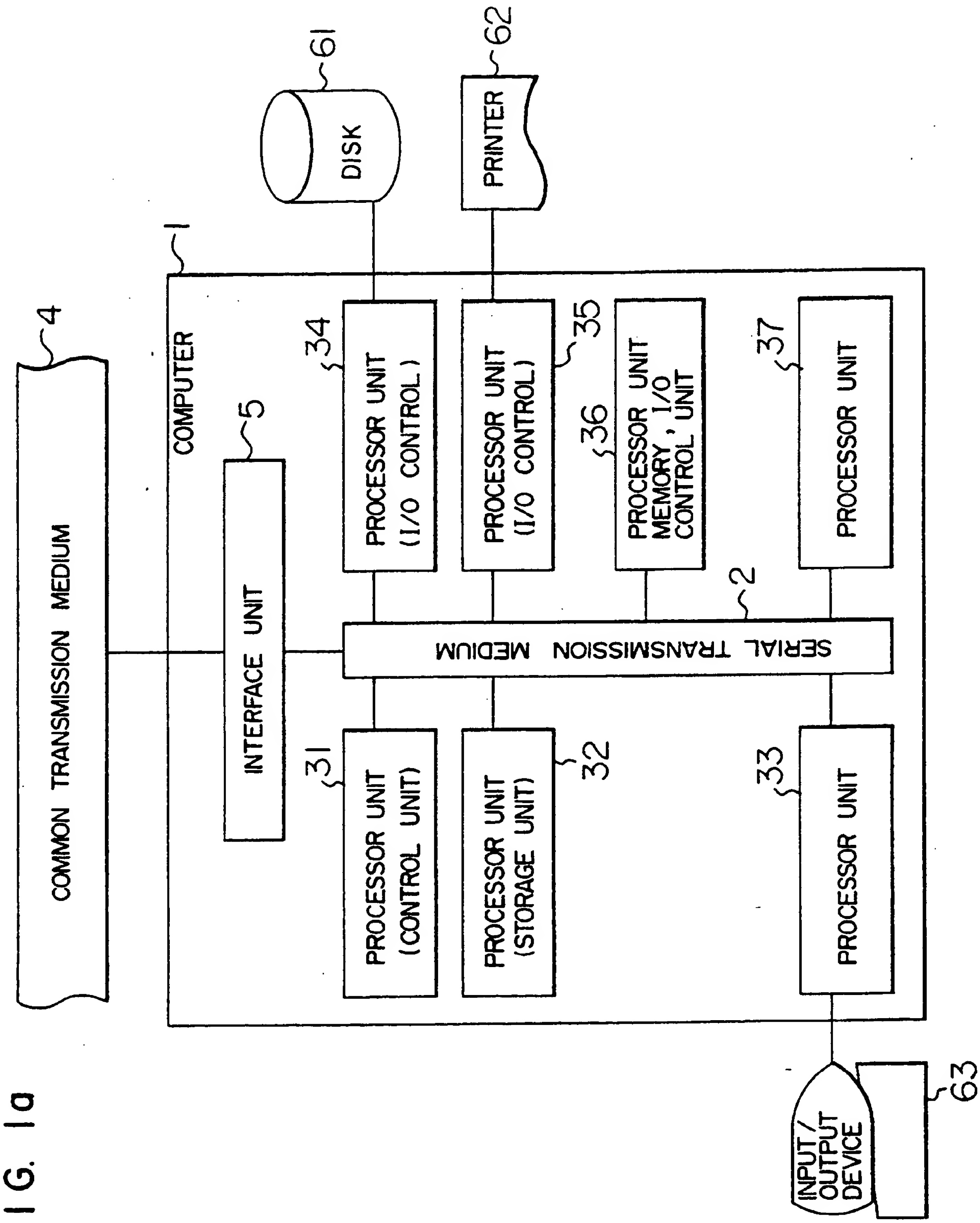
16. A loosely coupled multiprocessor computer as claimed in Claim 12, wherein a broadcast method is employed as the data transmission sequence effected via said serial transmission medium.

17. A loosely coupled multiprocessor computer as claimed in Claim 12, wherein said transmission control means sets a content code used for judging whether or not data broadcasted to said serial transmission medium is required, to said broadcasted data as said transmission data.

18. A loosely coupled multiprocessor computer as claimed in Claim 12, wherein a plurality of loosely coupled multiprocessor computers are connected via a common transmission medium with each other, and are equipped with an interface unit for controlling the data transmission performed via said common transmission medium.

19. A loosely coupled multiprocessor computer as claimed in Claim 12, wherein software management programs used in said process means and unit process means are identical to each other.

FIG. 1a


COMMON TRANSMISSION MEDIUM
4
COMPUTER
1
INTERFACE UNIT
5
SERIAL TRANSMISSION MEDIUM
2
PROCESSOR UNIT (CONTROL UNIT)
31
PROCESSOR UNIT (STORAGE UNIT)
32
PROCESSOR UNIT
33
PROCESSOR UNIT (I/O CONTROL)
34
PROCESSOR UNIT (I/O CONTROL)
35
PROCESSOR UNIT MEMORY, I/O CONTROL UNIT
36
PROCESSOR UNIT
37
DISK
61
PRINTER
62
INPUT/ OUTPUT DEVICE
63

F I G. 1b

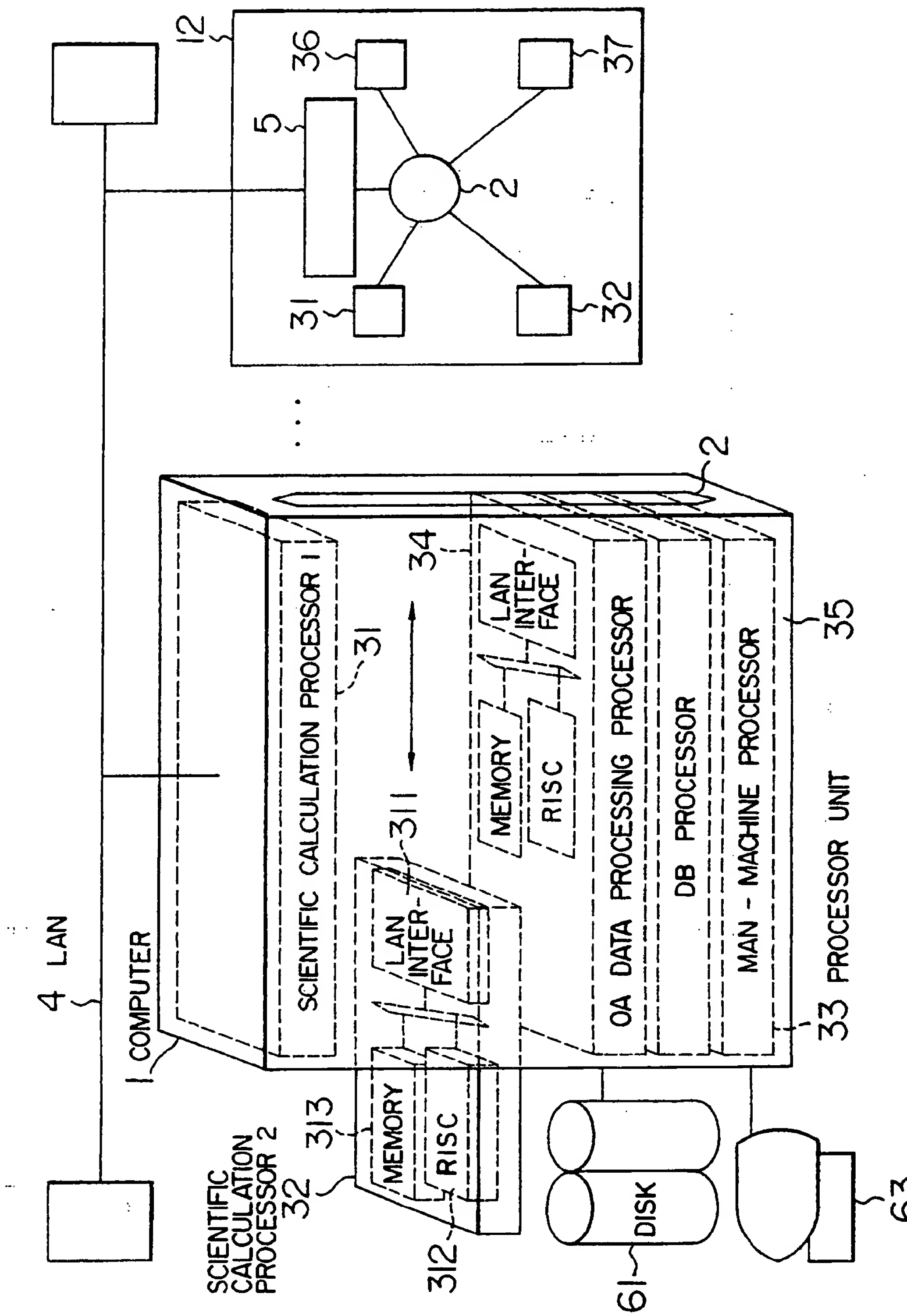
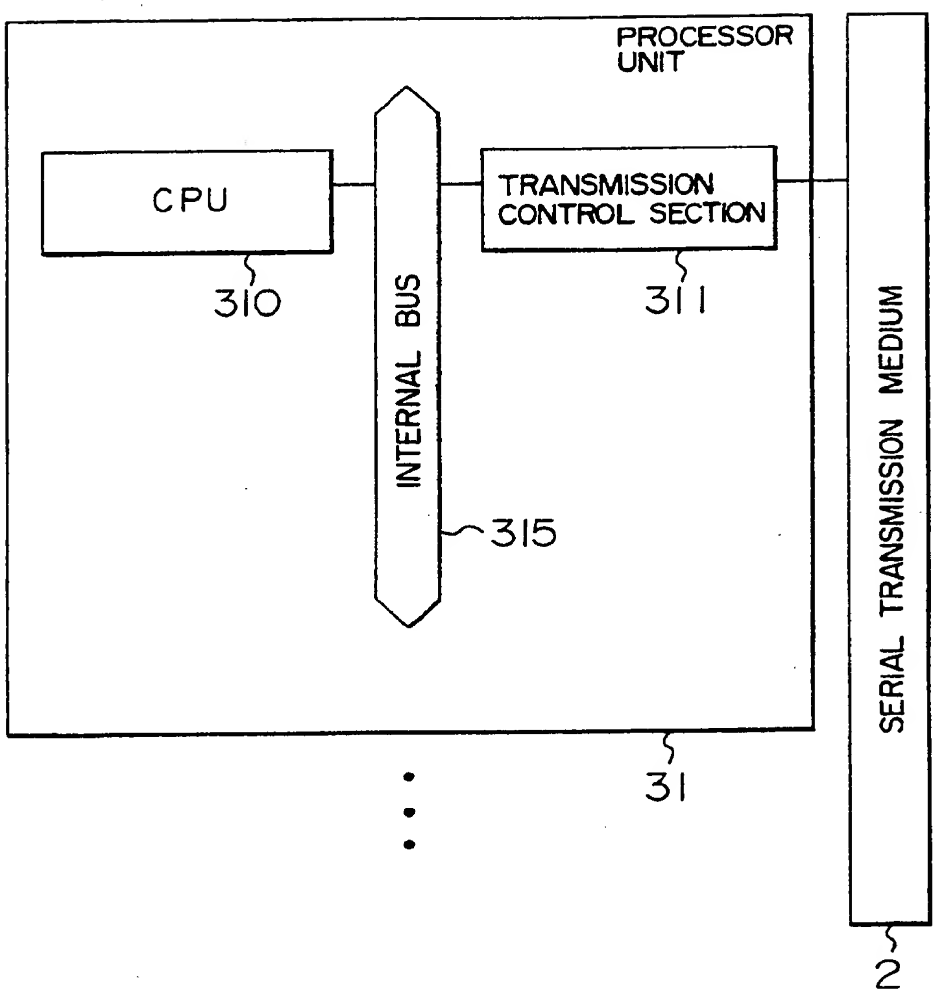

4 LAN
1 COMPUTER
SCIENTIFIC CALCULATION PROCESSOR 1
31
311
LAN INTER-FACE
MEMORY
RISC
34
OA DATA PROCESSING PROCESSOR
DB PROCESSOR
MAN - MACHINE PROCESSOR
33 PROCESSOR UNIT
35
2
SCIENTIFIC CALCULATION PROCESSOR 2
32
313
312
DISK
61
63
12
5
36
37
31
32

FIG. 2a


PROCESSOR UNIT
CPU
310
INTERNAL BUS
315
TRANSMISSION CONTROL SECTION
311
31
SERIAL TRANSMISSION MEDIUM
2

F I G. 2b

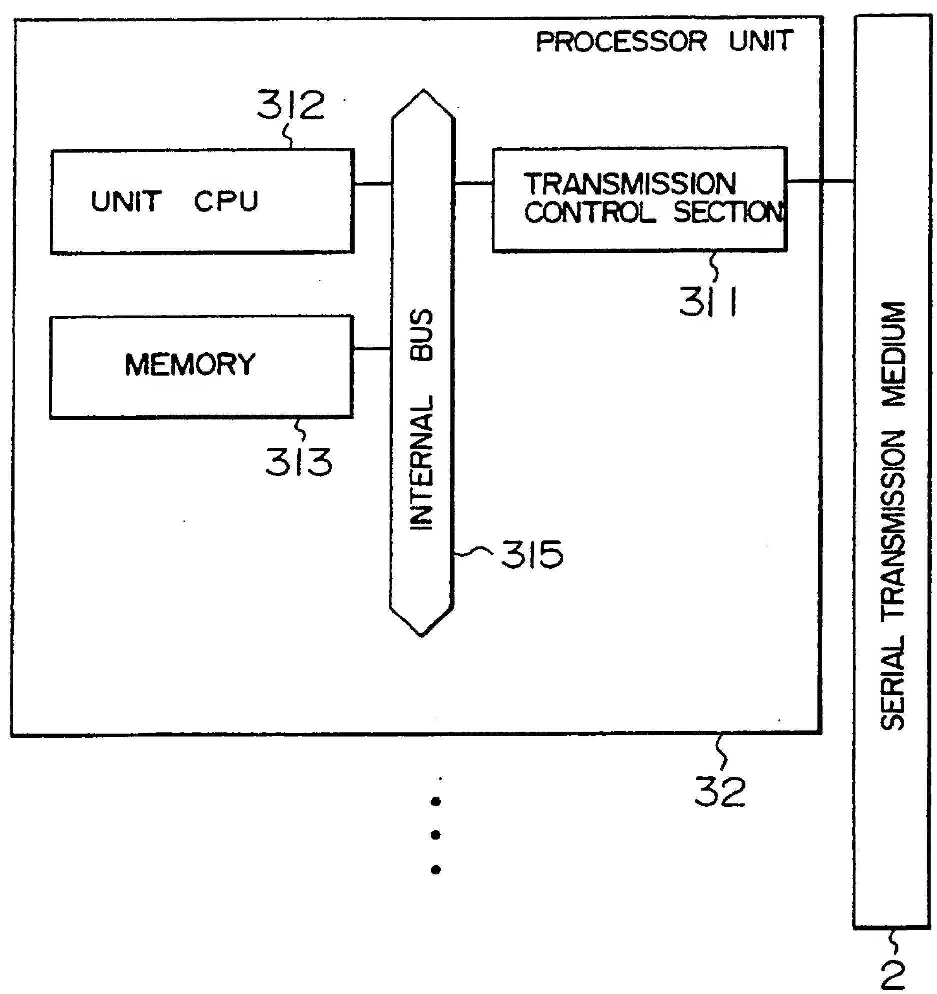

PROCESSOR UNIT
312
UNIT CPU
TRANSMISSION CONTROL SECTION
311
MEMORY
313
INTERNAL BUS
315
32
SERIAL TRANSMISSION MEDIUM
2

FIG. 2c

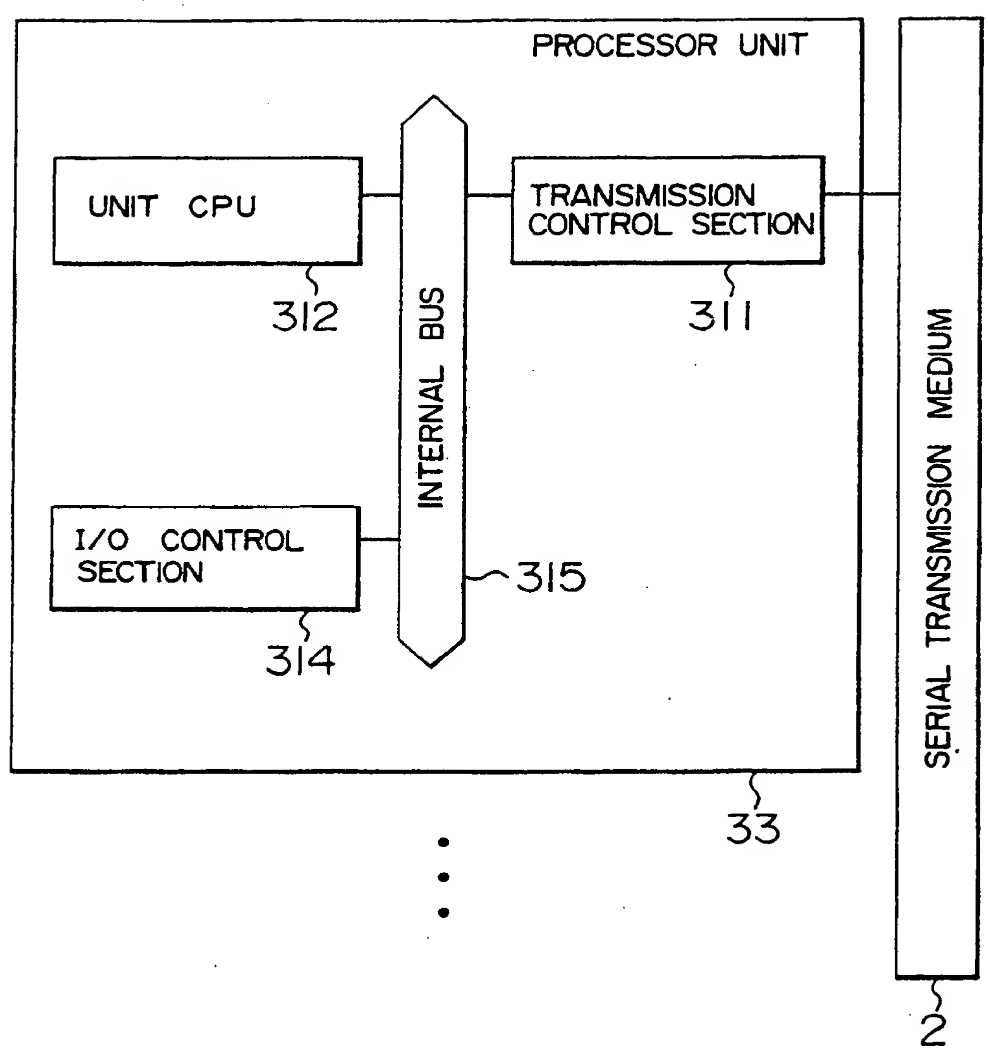
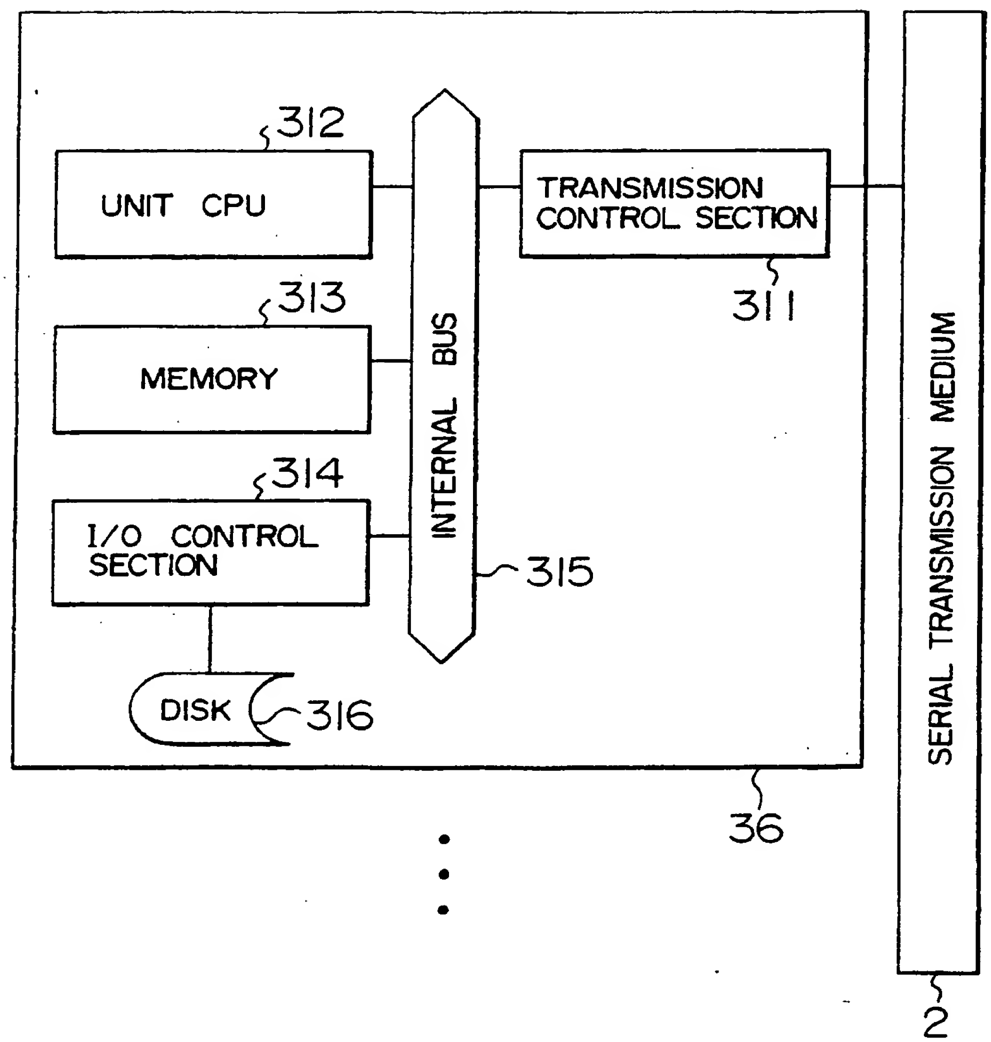
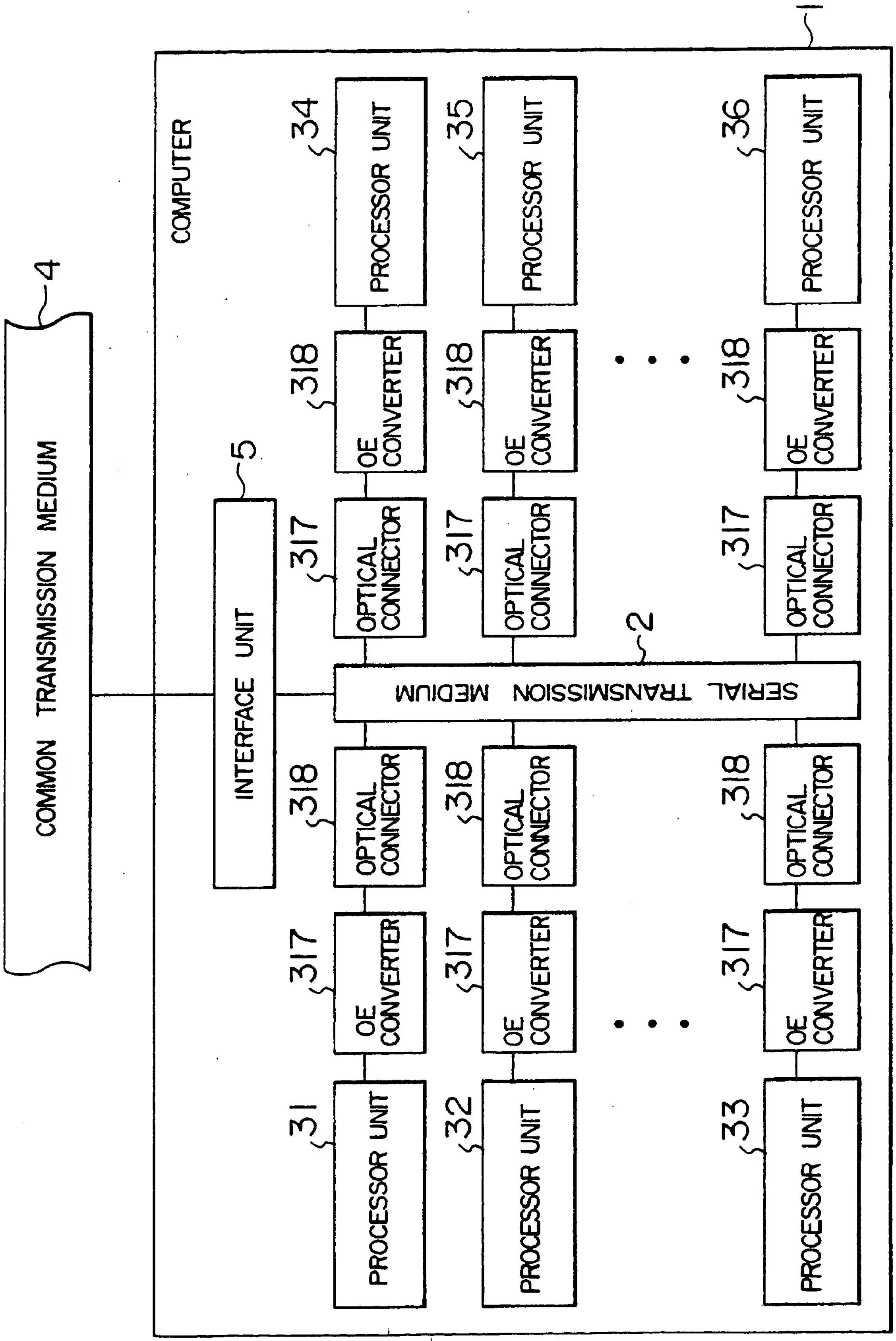

PROCESSOR UNIT
UNIT CPU
TRANSMISSION CONTROL SECTION
INTERNAL BUS
I/O CONTROL SECTION
SERIAL TRANSMISSION MEDIUM
312
311
315
314
33
2

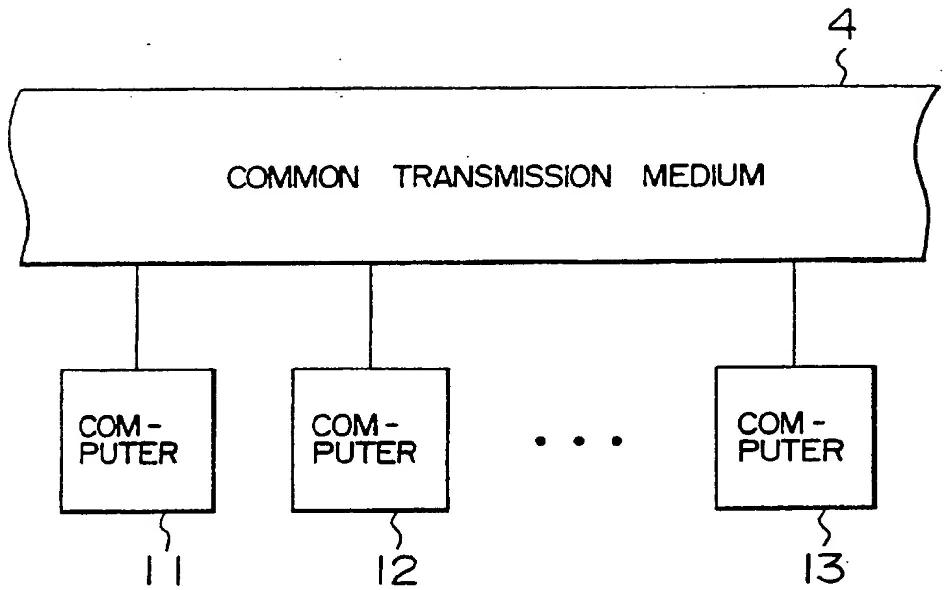
FIG. 2d


312
UNIT CPU
313
MEMORY
314
I/O CONTROL SECTION
DISK
316
INTERNAL BUS
315
TRANSMISSION CONTROL SECTION
311
36
SERIAL TRANSMISSION MEDIUM
2

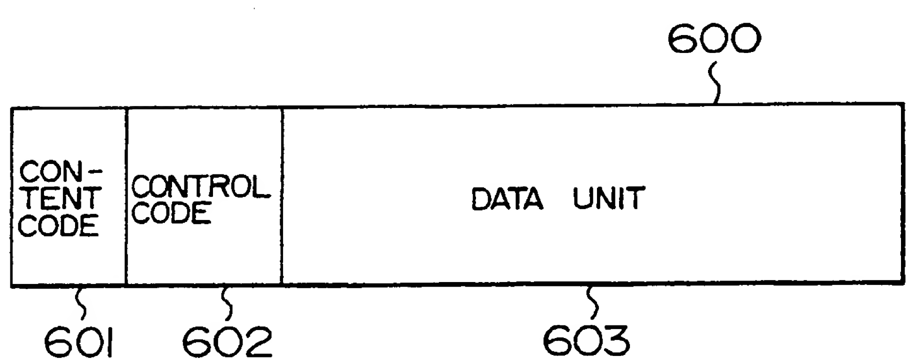
F I G. 3


COMMON TRANSMISSION MEDIUM
4
COMPUTER
1
INTERFACE UNIT
5
SERIAL TRANSMISSION MEDIUM
2
PROCESSOR UNIT
31
PROCESSOR UNIT
32
PROCESSOR UNIT
33
PROCESSOR UNIT
34
PROCESSOR UNIT
35
PROCESSOR UNIT
36
OE CONVERTER
317
OPTICAL CONNECTOR
318
OPTICAL CONNECTOR
317
OE CONVERTER
318

F I G. 4


4
COMMON TRANSMISSION MEDIUM
COM-PUTER
COM-PUTER
COM-PUTER
11
12
13

F I G. 5


600
CON-TENT CODE
CONTROL CODE
DATA UNIT
601
602
603

F I G. 6

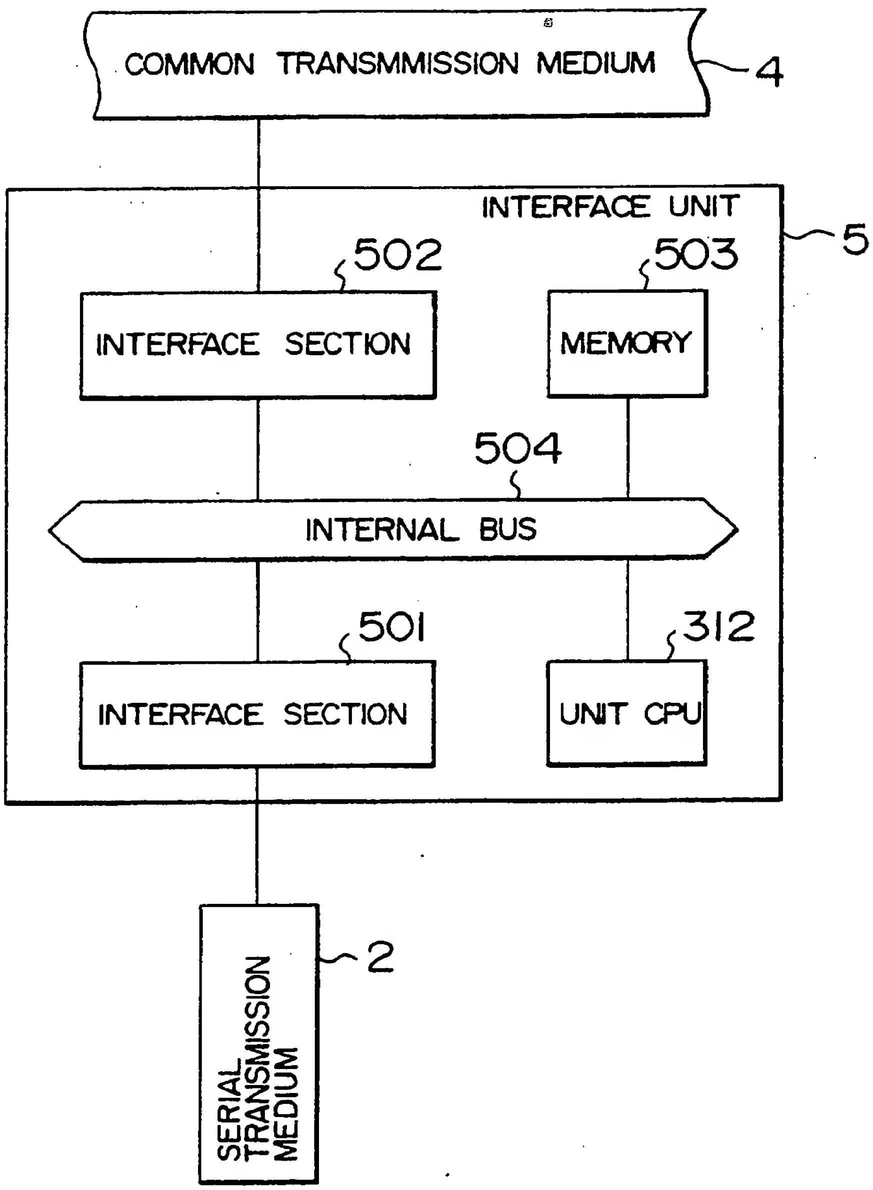
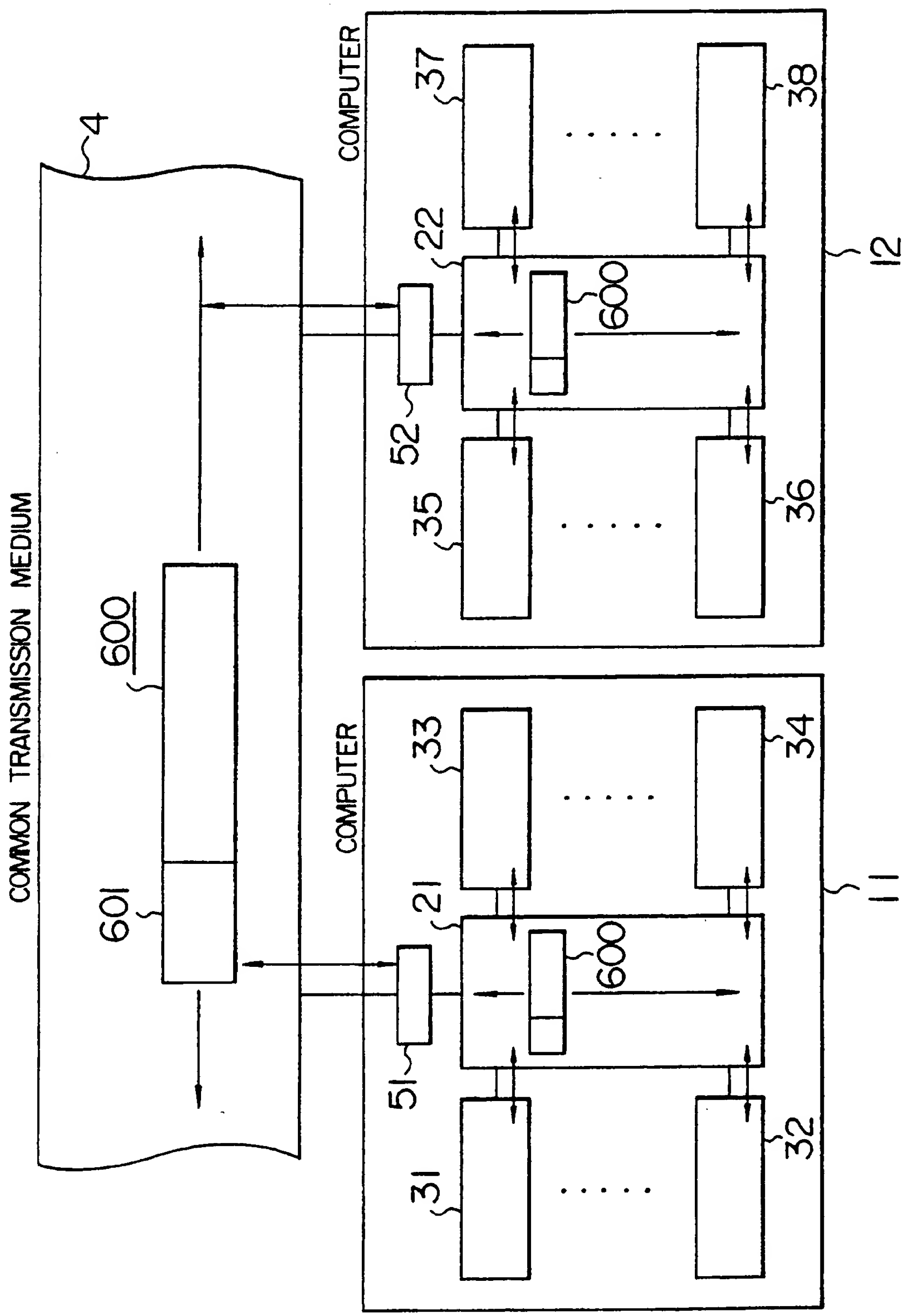
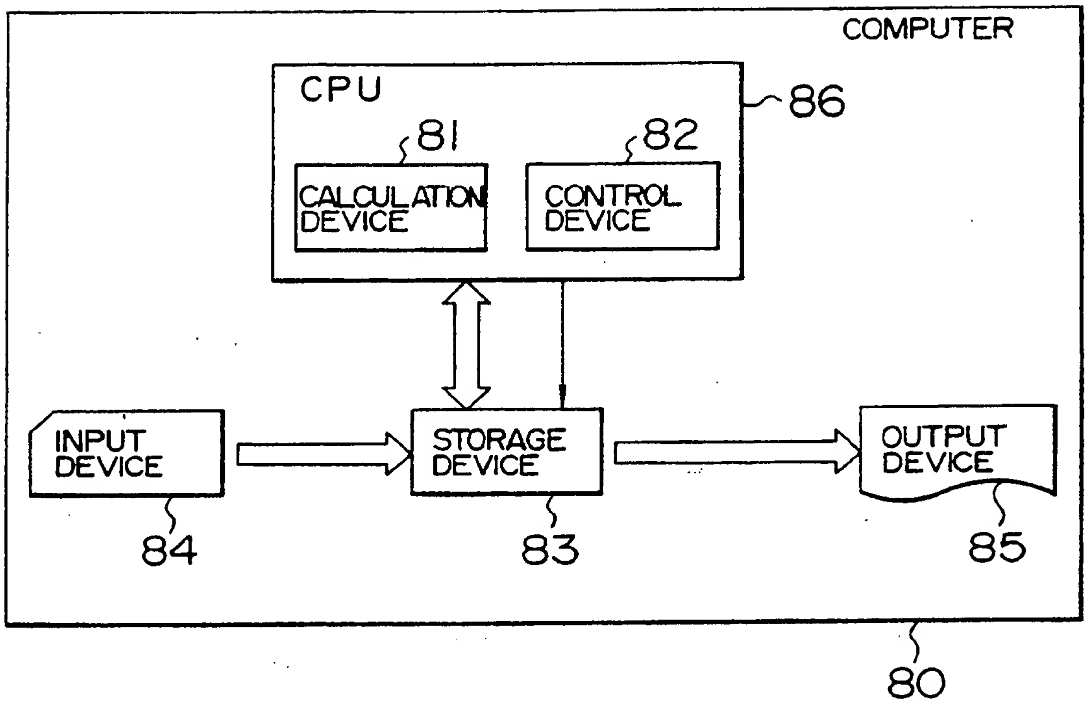

COMMON TRANSMMISSION MEDIUM
4
INTERFACE UNIT
5
502
503
INTERFACE SECTION
MEMORY
504
INTERNAL BUS
501
312
INTERFACE SECTION
UNIT CPU
2
SERIAL TRANSMISSION MEDIUM

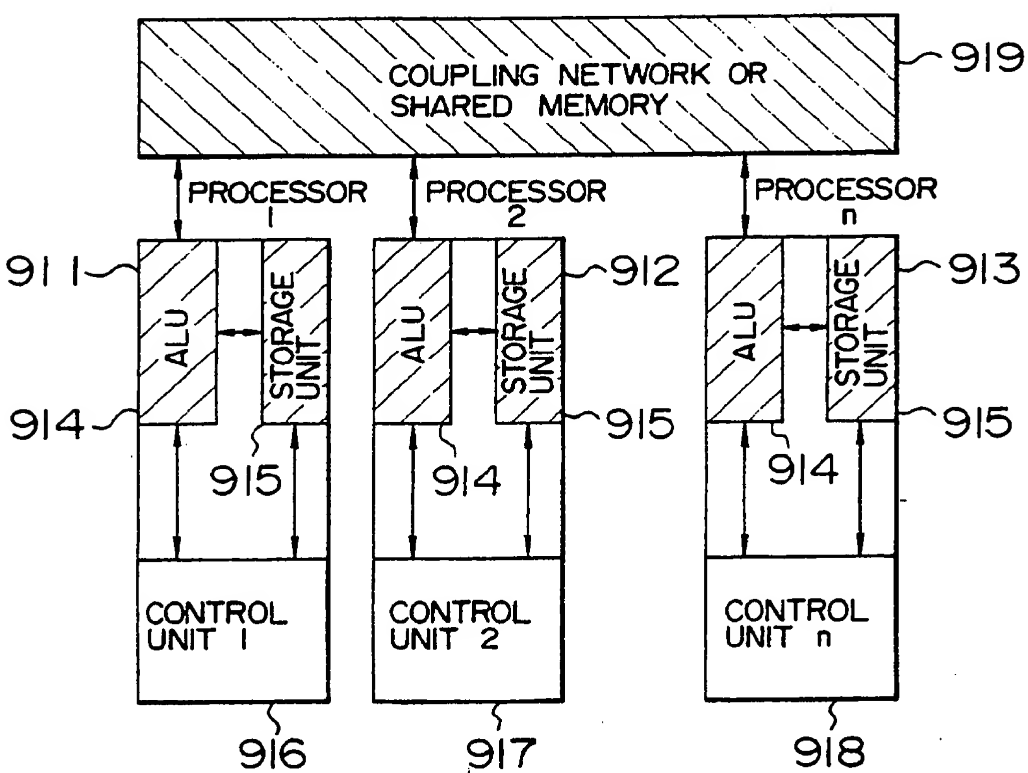
FIG. 7


COMMON TRANSMISSION MEDIUM
4
600
601
COMPUTER
COMPUTER
11
12
21
22
600
600
31
32
33
34
35
36
37
38
51
52

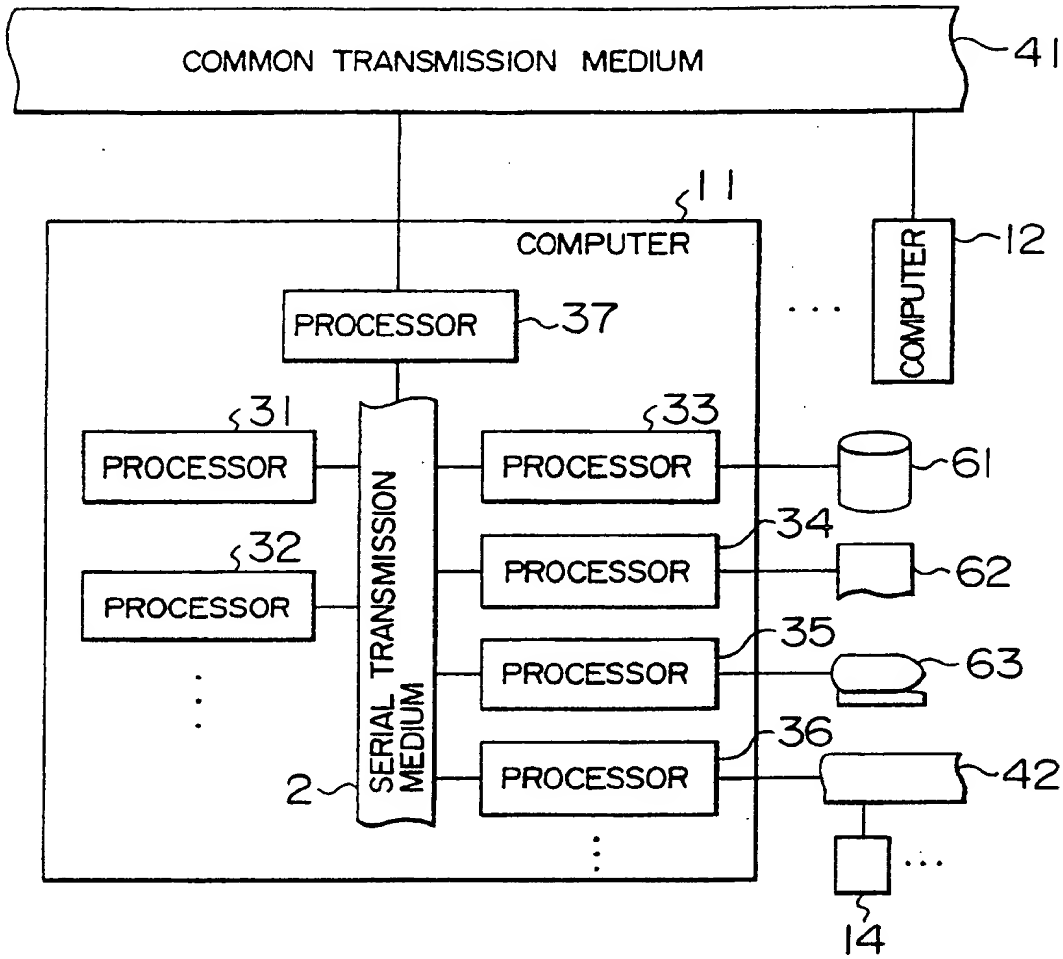
F I G. 8 PRIOR ART



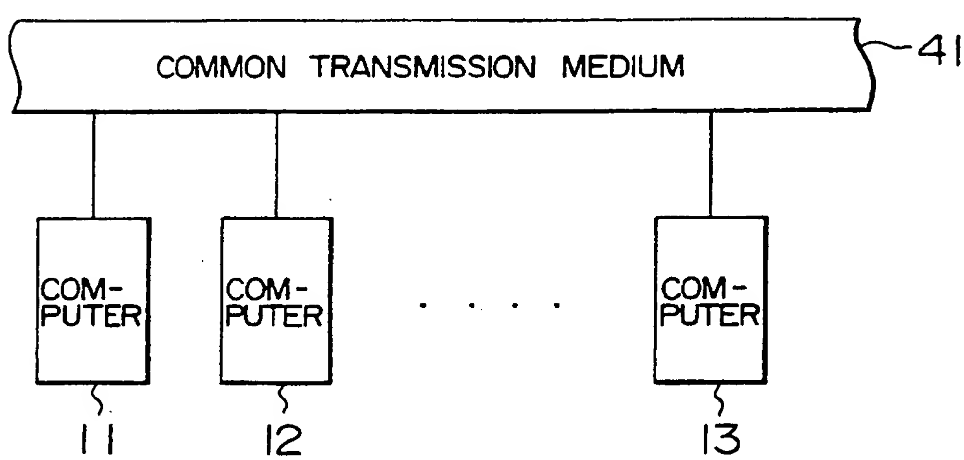
F I G. 9



F I G. 10


COMMON TRANSMISSION MEDIUM
41
11
COMPUTER
12
COMPUTER
PROCESSOR
37
31
PROCESSOR
33
PROCESSOR
61
34
PROCESSOR
62
32
PROCESSOR
35
PROCESSOR
63
SERIAL TRANSMISSION MEDIUM
36
PROCESSOR
42
2
14

F I G. 11


COMMON TRANSMISSION MEDIUM
41
COM-PUTER
COM-PUTER
COM-PUTER
11
12
13

F I G. 12

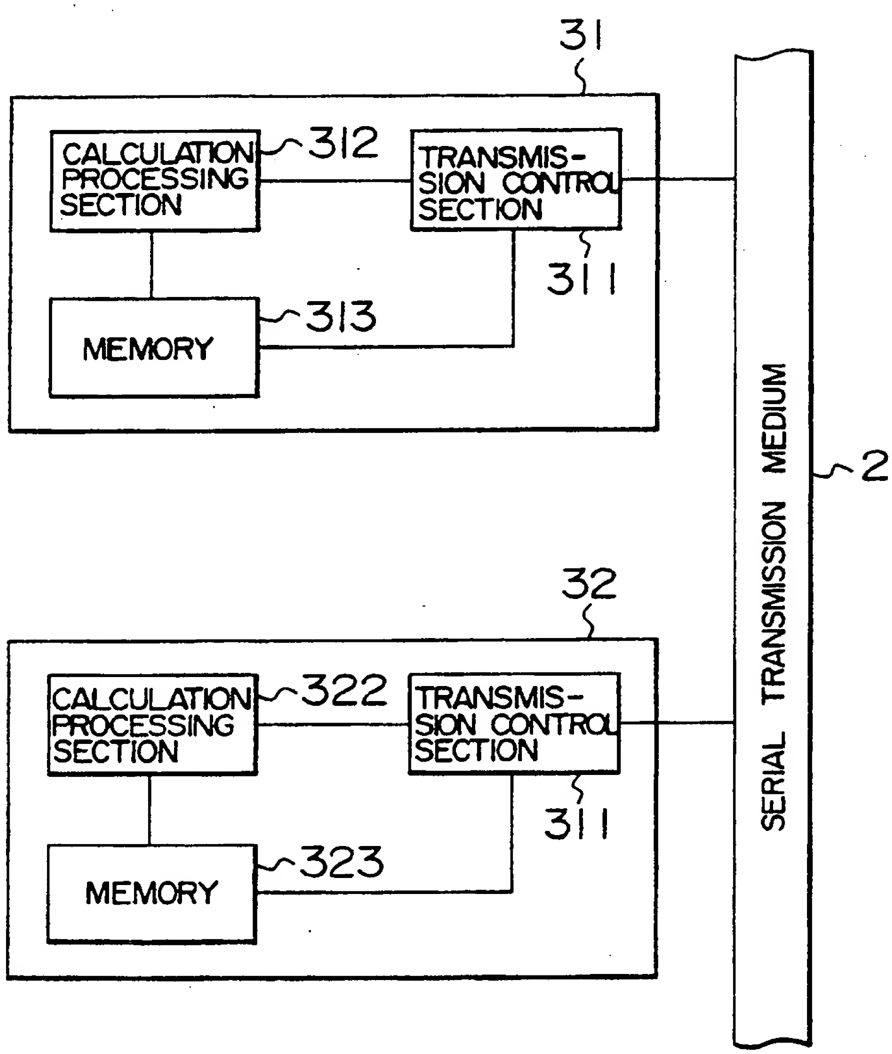

31
CALCULATION PROCESSING SECTION
312
TRANSMISSION CONTROL SECTION
311
MEMORY
313
32
CALCULATION PROCESSING SECTION
322
TRANSMISSION CONTROL SECTION
311
MEMORY
323
SERIAL TRANSMISSION MEDIUM
2

FIG. 13

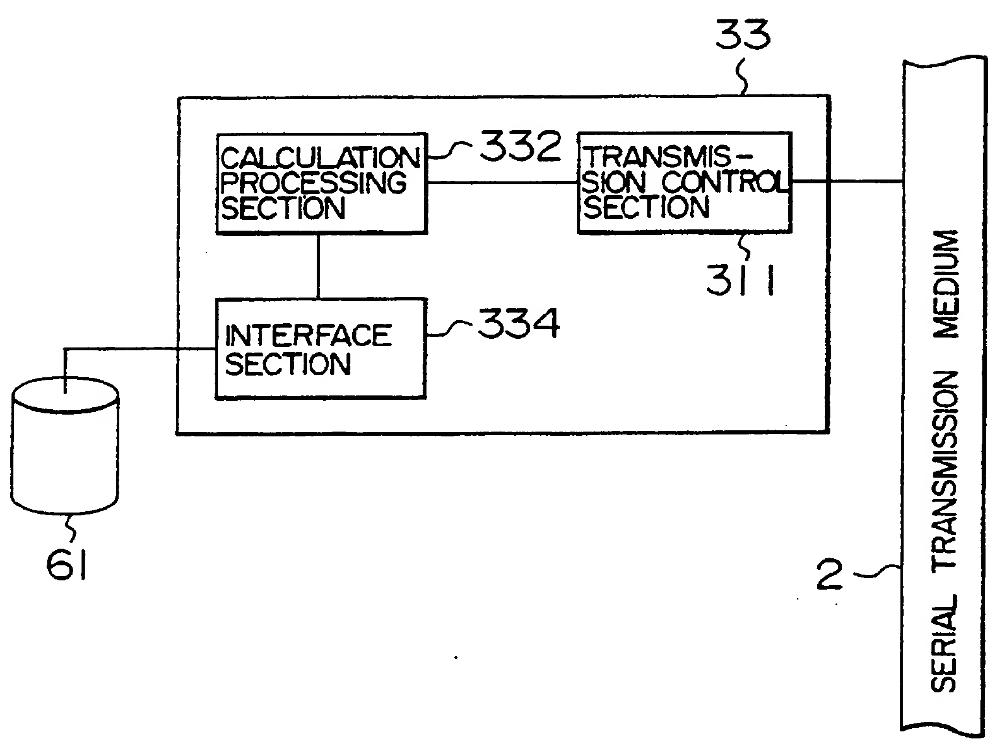
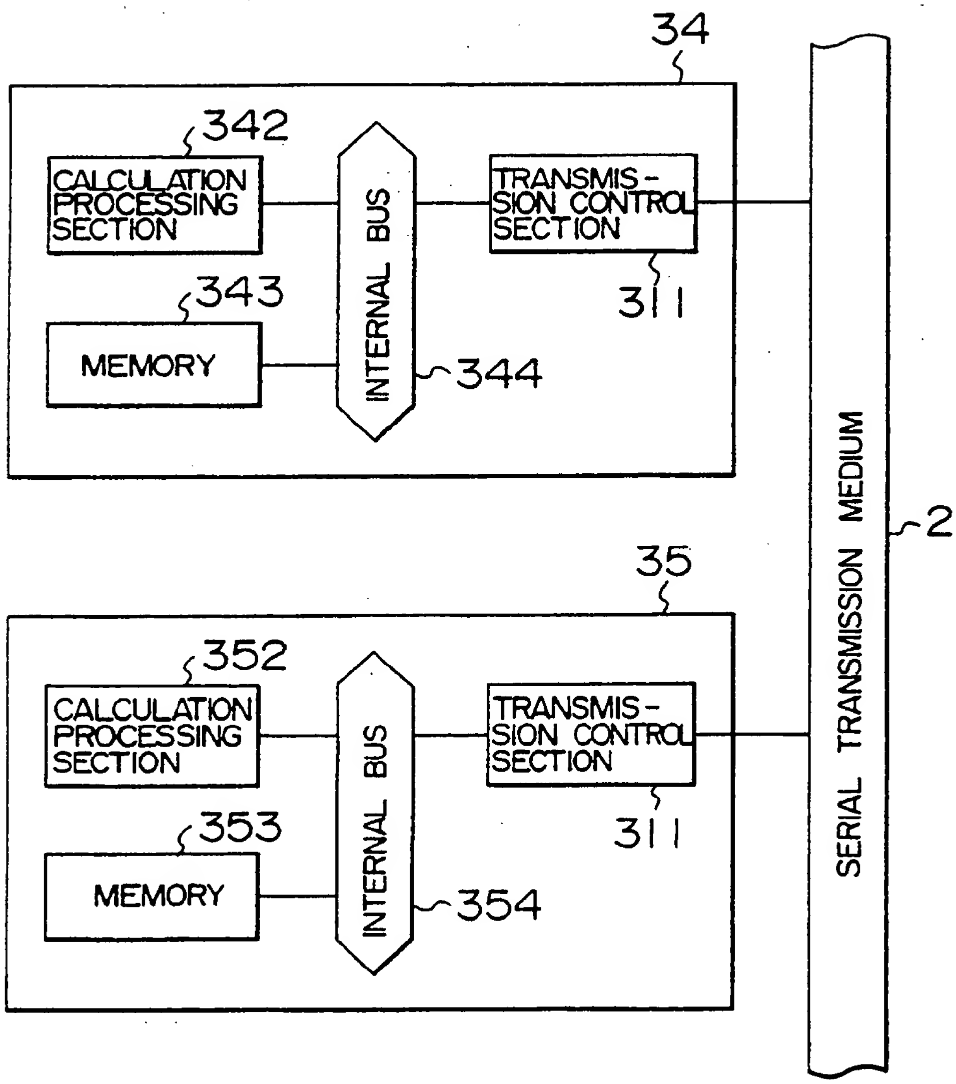
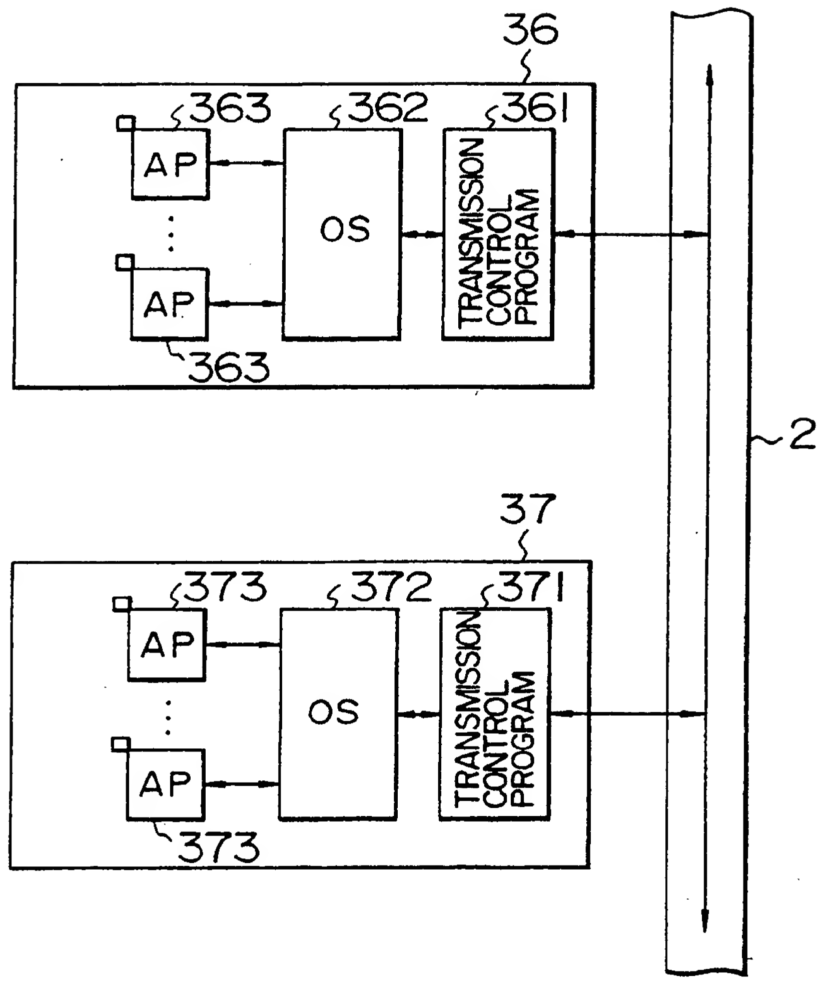

33
CALCULATION PROCESSING SECTION
332
TRANSMISSION CONTROL SECTION
311
INTERFACE SECTION
334
61
2
SERIAL TRANSMISSION MEDIUM

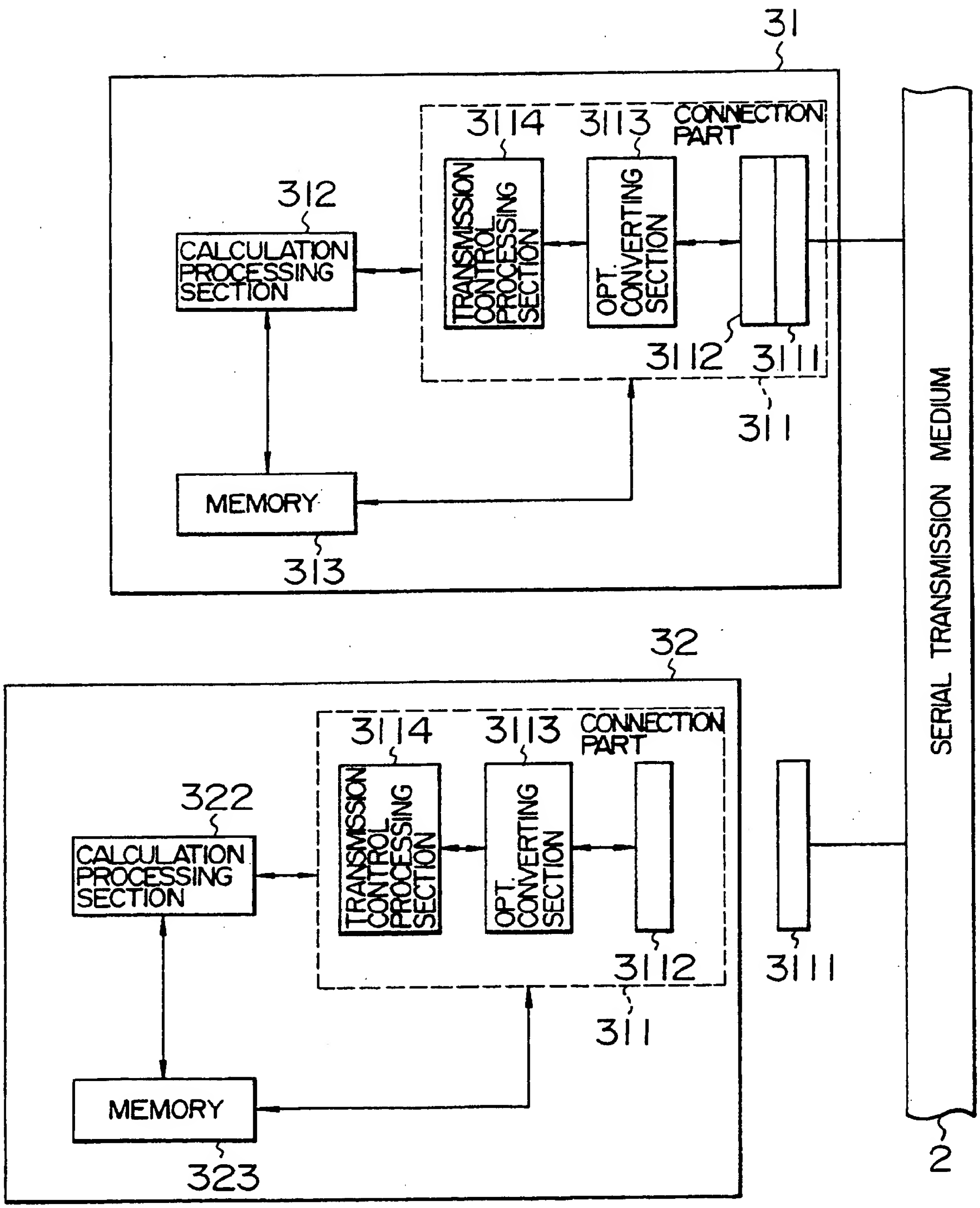
FIG. 14


34
342
CALCULATION PROCESSING SECTION
343
MEMORY
INTERNAL BUS
344
TRANSMIS-SION CONTROL SECTION
311
35
352
CALCULATION PROCESSING SECTION
353
MEMORY
INTERNAL BUS
354
TRANSMIS-SION CONTROL SECTION
311
SERIAL TRANSMISSION MEDIUM
2

F I G. 15


36
363
362
361
AP
OS
TRANSMISSION CONTROL PROGRAM
AP
363
2
37
373
372
371
AP
OS
TRANSMISSION CONTROL PROGRAM
AP
373

F I G. 16


31
3114
3113
CONNECTION PART
312
CALCULATION PROCESSING SECTION
TRANSMISSION CONTROL PROCESSING SECTION
OPT. CONVERTING SECTION
3112
3111
311
MEMORY
313
SERIAL TRANSMISSION MEDIUM
32
3114
3113
CONNECTION PART
322
CALCULATION PROCESSING SECTION
TRANSMISSION CONTROL PROCESSING SECTION
OPT. CONVERTING SECTION
3112
3111
311
MEMORY
323
2